



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

17

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/636,591	08/10/2000	Shuhei Kato	P100341-00003	6504
4372	7590	10/18/2007		
ARENT FOX LLP 1050 CONNECTICUT AVENUE, N.W. SUITE 400 WASHINGTON, DC 20036			EXAMINER LAO, LUN S	
			ART UNIT 2615	PAPER NUMBER
			NOTIFICATION DATE 10/18/2007	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

DCIPDocket@arentfox.com
IPMatters@arentfox.com
Patent_Mail@arentfox.com

Office Action Summary

Application No.

09/636,591

Applicant(s)

KATO ET AL.

Examiner

Lun-See Lao

Art Unit

2615

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 6-14 is/are rejected.
- 7) ☒ Claim(s) 4 and 5 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

Introduction

1. This action responds to the amendment filed on 08-09-2007. Claim 3 has been amended. Claims 1-14 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3 and 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malcolm (US Pat. 6,373,954) in view of Tsukamoto et al. (US PAT. 4,815,352).

Consider claim 1, Malcolm teaches a sound processor formed on a single semiconductor device to reproduce pulse-code-modulated sound waveform data, comprising (see abstract):

sequence control means (see fig.1A, 121, 122,120, such as first in, first out and see col. 11 line 57-62);

bus interface means (101) for a common bus including an address bus and a data bus;

bus master means (103) for issuing an address to said common bus through said bus interface means (101) under control of said sequence control means (103), and reading and writing data for a resource connected to said common bus; data holding means

Art Unit: 2615

(103) for holding part of data read out by said bus master means (103); M sets (M being a natural number) of independent digital/analog converting means ((110) for converting digital data over a sound channel into an analog sound signal;

data output control means (118, DSP) for controlling an output of data to said digital/analog converting means (110 and see col. 10 line 28-col.11 line 62); but Malcolm does not clearly teach that time division multiplexing means for time-division-multiplexing and outputting data of over N sets (N being a natural number greater than 2) of sound channels to each of digital/analog converting means required for reproduction; whereby data is to be simultaneously reproduced over a plurality of sets of sound channels represented by a product of M and N.

However, Tsukamoto teaches that time division multiplexing means (see fig.17, 6-7) for time-division-multiplexing and outputting data of over N sets (N being a natural number greater than 2) of sound channels to each of digital/analog converting means (91-93) required for reproduction (see abstract and col.8 lines 15-55); whereby data is inherently to be simultaneously reproduced over a plurality of sets of sound channels represented by a product of M and N (see fig.17 and col.16 line 20-62).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Tsukamoto in to Malcolm so that a plurality of the wave data are provided in a time division multiplex form from said wave memory through the time division multiplex calculation by said address calculator for the wave memory to improve the sound quality.

Art Unit: 2615

Consider claim 2, Malcolm teaches a sound processor of bus master means (see fig.1A, 103) further has a function of determining whether data required in reproduction is stored in said data holding means or not, and acquiring the data from a resource connected to said common bus and storing the data in said data holding means (103) where the data required in reproduction is not stored in said data holding means (103 and see col10 line 28-58).

Consider claim 3 Tsukamoto teaches a sound processor of the digital/analog converting means (see fig.17, 91-93) is structured by a plurality of digital/analog converters and said digital/analog converters are in cascade connection (see fig.17).

Consider claim 8-9, Tsukamoto teaches a sound processor of the data output means (see fig. 17) further has a function of outputting data in later timing, with respect to timing (6,7) of outputting data to a certain digital/analog converter (91-93), to a digital/analog converter connected in a next stage thereto, and controlling timing (by microcomputer) of outputs to eliminate interference between time slots due to signal delay between said cascade-connected digital/analog converters (91-93) when outputting data to said cascade-connected digital/analog converter (91-93 and see col.16 line 20-col.16 line 61) and a sound processor of the data output control means (microcomputer) is to be programmably set in timing of outputting data (see col. 16 line 20-col.17 line 61).

Consider claim 10-12, Malcolm teaches a sound processor of the sound waveform data is configured by two arrays (array0 and array1 and see table 67) having end codes provided at respective terminal ends of the arrays (see col.120 line 35-col.121 line 62),

Art Unit: 2615

and said bus master means (see fig.1A, 103) further having a function to start reading at a head of the first array (array0), uninterruptedly starting reading at a head of the second array (array1) immediately after reading the end code of the first array (array0), and uninterruptedly starting reading at the head of the second array (array1) after reading out the end code of the second array (array1 and see col.119 line 19 –col. 122 line 63); and a sound processor of further comprising accumulating means (see fig.3, 315) and means (see fig. 45) for storing pitch control information (by microcontroller), wherein the pitch control information is read out at a constant time interval (see col.119 line 19-67) and accumulated by said accumulating means (see fig.3, 315), and one part or the whole of an accumulation result being utilized as address information for access to a common bus of said bus master means (see fig.1A,103 and col.12 line 41-col.13 line 26); and a sound processor of the bus interface means (see fig.1, 101) is provided independent for a plurality of common buses.

Consider claim 13, Malcolm teaches a sound processor of further comprising interrupt request control means (see fig.1, 103 and col. 38 line 42-67) to be controlled by said sequence control means(see fig.1 121, 122,120, such as first in, first out and see col. 11 line 57-62); and generate an interrupt request signal, wherein said bus master means (see fig.1A, 103) comprises waveform reading control means (see fig. 43L, 430 and col. 108 line 60-col.111 line 67) to control reading of sound waveform data, envelope/preset control means (see fig.1, 103) to control reading out of parameters for controlling envelope data and sound reproduction (see col. 119 line 19-67), and

Art Unit: 2615

access arbitrating means (microcontroller and software) an to arbitrate between an access of from said envelope/preset control means to the common bus and an access of from said waveform reading control means (microcontroller) to the common bus (see col. 99 line 7-51 and col.119 line 19-col.120 line 67),

said bus interface means (see fig.1A, 101) comprising

first bus interface means (101) to a first common bus, and

second bus interface (109) to a second common bus (see col.10 line 20-64).

Consider claim 14, Malcolm teaches a sound processor apparatus, comprising:

being configured on one single semiconductor device (see abstract),

first and second buses (see fig.1, 101,105) having independent data transfer capabilities,

a central processing unit (see fig1, 103 microcontroller) and a sound processor (118, DSP) according (see col.10 line 28-64) to claim 12 or 13 (see previous rejection claim 1 and claim 12 or 13) as bus masters (see fig.1, 101) for said first and second buses, a memory connected to said first bus, a first bus arbitrating means (see fig.1A, 101) to administer arbitration over said first bus (see col. 10 line 28-65), and a second bus arbitrating means (109) to administer arbitration over said second bus (109, and see col.10 line 50-65).

4. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malcolm (US Pat. 6,373,954) as modified by Tsukamoto et al.(US PAT. 4,815,352) as applied to claim 1 above, and further in view of Anderson (US PAT. 6,078,594).

Art Unit: 2615

Consider claim 6, Malcolm and Tsukamoto do not clearly teach a sound processor of the data output control means further has a function to control a constant period of a mute state between adjacent sound channels time-division-multiplexed.

However, Anderson teaches a sound processor of the data output control means further has a function to control a constant period of a mute state between adjacent sound channels time-division-multiplexed (see col.11 lines 35-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Anderson into the teaching of Malcolm and Tsukamoto to provide to the latency of channel changes through the use of flags that are passed with the data between the transport demultiplexor and decoder.

Consider claim 7, Anderson teaches a sound processor of the mute state has a period to be set programmable (see col.6 line 27-51).

Allowable Subject Matter

5. Claims 4-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 08-09-2007 have been fully considered but they are not persuasive.

Art Unit: 2615

Applicant argued that Malcolm neither discloses nor suggests that FM synthesis circuit 116 controls sequences in which the "bus master means" 101 issues addresses to a common bus (see the remarks page 11, 3rd paragraph).

The examiner disagrees. Malcolm discloses bus master means (103 in fig. 1A) for issuing an address to said common bus through said bus interface means (101) under control of said sequence control means (103 and see col. 10 line 28-col.11 line 62). It meets the limitation as recited in claim 1.

Applicant argued that Tsukamoto neither discloses nor suggests a cascade connection of the three D/As disclosed therein (see remarks page 13, last paragraph).

The examiner disagrees. Tsukamoto neither discloses a cascade connection of the three D/As (in parallel cascade connection and see fig.17). It meets the limitation as recited in claim 3.

Applicant further argued that the Office Action asserts that Malcolm teaches the claimed first and second buses by ISA bus interface 101 and joystick logic 105. See Office Action, p. 7. However, joystick logic 105 does not comprise a second bus (see remarks page 14, second paragraph).

The examiner disagrees. Malcolm teaches the claimed first and second buses by ISA bus interface 101 and joystick logic 105 which joystick logic 105 comprises a second bus (serial bus).

However, Malcolm teaches a central processing unit (see fig1, 103 microcontroller) and a sound processor (118, DSP) according (see col.10 line 28-64) to claim 12 or 13 (see previous rejection claim 1 and claim 12 or 13) as bus masters (see fig.1, 101) for

Art Unit: 2615

said first and second buses, a memory connected to said first bus, a first bus arbitrating means (see fig.1A, 101) to administer arbitration over said first bus (see col. 10 line 28-65), and a second bus arbitrating means (109) to administer arbitration over said second bus (109, and see col.10 line 50-65). It meets the limitation as recited in claim 14.

Applicant further argued to establish prima facie obviousness of a rejected claim, the applied art of record must teach or suggest each feature of a rejected claim. See M.P.E.P. §2143.03 and *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998). As explained above, none of the applied art of record, either alone or in combination, teaches or suggests each and every feature recited in independent claims 1 and 14 (see remarks page 14 3rd paragraph).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, The combination of Malcolm and Tsukamoto, they both teach microcontroller for the audio processing system with the D/A. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Tsukamoto in to Malcolm so that a plurality of the wave data are provided in a time division multiplex

Art Unit: 2615

form from said wave memory through the time division multiplex calculation by said address calculator for the wave memory to improve the sound quality.

Conclusion

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Matthews (US PAT. 6,314,330) are recited to show other related the sound processor.

9. Any response to this action should be mailed to:

Mail Stop ____ (explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Facsimile responses should be faxed to:

Art Unit: 2615

(703) 872-9306

Hand-delivered responses should be brought to:

Customer Service Window

Randolph Building

401 Dulany Street


Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lao,Lun-See whose telephone number is (571) 272-7501. The examiner can normally be reached on Monday-Friday from 8:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chin Vivian, can be reached on (571) 272-7848.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 whose telephone number is (571) 272-2600.

Lao,Lun-See L.S.
Patent Examiner
US Patent and Trademark Office
Knox
571-272-7501
10-11-2007


VIVIAN CHIN
SUPERVISOR PATENT EXAMINER
TECHNOLOGY CENTER 2600